PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

#13B Amdt
M. Brinson
2/25/03

In re application of

Docket No: Q62964

Fumihiko HAYASHI

Appln. No.: 09/864,259

Group Art Unit: 2814

Confirmation No.: 3213

Examiner: Hoai V. PHAM

Filed: May 25, 2001

For: SEMICONDUCTOR DEVICE HAVING A MEMORY CELL REGION AND A PERIPHERAL CIRCUIT REGION AND METHOD OF MANUFACTURING THEREOF

RESPONSE TO ELECTION/RESTRICTION AND AMENDMENT UNDER 37 C.F.R. § 1.111

Commissioner for Patents
Washington, D.C. 20231

Sir:

In further response to the Office Action dated May 6, 2002 and to the Examiner's communication of December 16, 2002 informing Applicant that the response filed on September 26, 2002 was non-responsive, please amend the above-identified application as follows:

IN THE CLAIMS:

Please add the following new claims:

31. A method of manufacturing a semiconductor memory device, comprising:

selectively forming in a semiconductor substrate first, second and third diffusion regions apart from one another, said first and second diffusion regions constituting a first memory cell having a first floating gate over a first channel region sandwiched between said first and second

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